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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,843	07/21/2003	Veronika Polei	P2002,0618	6526

24131 7590 06/01/2005

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EXAMINER	
NGUYEN, KHIEM D	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 06/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/623,843	POLEI ET AL.
	Examiner	Art Unit
	Khiem D. Nguyen	2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4-7* is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on March 21st, 2005 has been entered. A new rejection is made as set forth in this Office Action. Claims (1-7) are pending in the application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

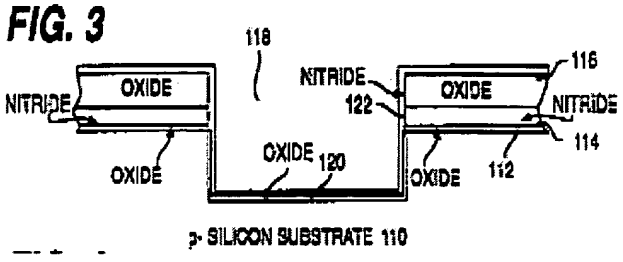
A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Horak et al. (U.S. Patent 6,063,658).

In re claim 1, **Horak** discloses a method for fabricating a buried bit line for a semiconductor memory, which comprises: producing strip-like doped regions parallel to and at distances from one another in a semiconductor body **110**, the regions being adapted to act as bit lines and as source/drain regions of a respective memory transistor (col. 5, line 60 to col. 6, line 23 and FIG. 3);

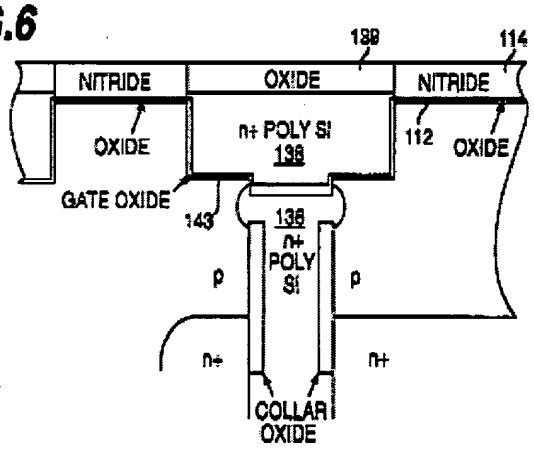
FIG. 3



applying laterally with respect to the doped regions, in each case, one layer sequence adapted to act as a gate dielectric (ONO) and including a lower boundary layer (oxide) **112**, a storage layer (nitride) **114**, and an upper boundary layer (oxide) **116** (col. 6, lines 23-34 and FIG. 3);

forming an oxide region **139** in each case on a side of the doped regions remote from the semiconductor body **110**, the oxide region **139** being thicker than the lower boundary layer **112** (col. 7, lines 18-36 and FIG. 6);

FIG.6

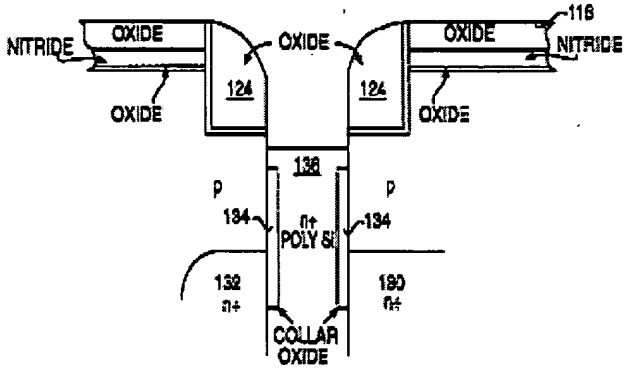


before the upper boundary layer **116** is applied, and after the application of the storage layer **114**, applying a sacrificial layer made from a material selectively etchable with respect to a material of the storage layer and to polysilicon onto the storage layer (col. 7, lines 18-24);

producing openings **118** in the sacrificial layer, the storage layer **114**, and the lower boundary layer **112**, extending the semiconductor body **110**, by using a mask (col. 6, lines 34-65);

introducing doped polysilicon **(n+ POLY Si)** into the openings **118** (col. 6, line 66 to col. 7, line 9 and FIG. 5);

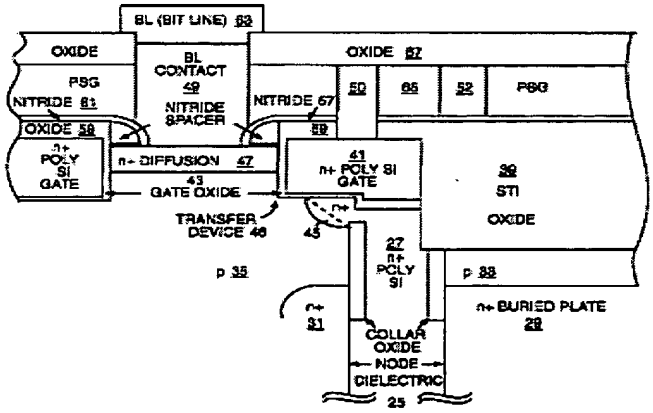
FIG. 5



removing the sacrificial layer (col. 7, lines 18-28); and

producing the upper boundary layer **116** on the storage layer **114** and oxidizing at least a proportion of the polysilicon to form the oxide region (col. 6, lines 23-34 and FIGS. 6 and 8).

FIG. 8



In re claim 2, **Horak** discloses that the sacrificial layer is produced as a deposited oxide (col. 7, lines 18-24).

In re claim 3, **Horak** discloses that the method according claim 1, which further comprises selecting the storage layer **114** from a group of materials consisting of silicon nitride, tantalum oxide, hafnium oxide, hafnium silicate, titanium oxide, zirconium oxide, aluminum oxide, and intrinsically conductive silicon (col. 6, lines 23-34).

Allowable Subject Matter

Claims 4-7 are allowed.

Response to Applicants' Amendment and Arguments

Applicants contend that according to the method of the instant application, the oxide region (6) is produced after the application of the lower boundary layer (3) and the storage layer (4), whereas the corresponding layers of Palm et al. can only be applied after the hard mask 16 and the spacers 17.

In response to Applicants' contention that, according to the method of the instant application, the oxide region (6) is produced after the application of the lower boundary layer (3) and the storage layer (4), whereas the corresponding layers of Palm et al. can only be applied after the hard mask 16 and the spacers 17. Examiner respectfully submits that the Applicants' argument is moot in view of the newly discovered reference to Horak et al. (U.S. Patent 6,063,658), applied under 35 U.S.C. 102(b) rejection presented in this Office Action (see pages 2-4).

For this reason, Examiner holds the rejection proper.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D. Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:30 AM - 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

K.N.
May 26th, 2005

W. DAVID COLEMAN
PRIMARY EXAMINER